Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 34-37 as follows:

Listing of Claims:

1. (Previously Presented) A memory hub, comprising:

a decoder being operable to receive memory requests including local memory requests directed to memory devices connected directly to the memory hub and remote memory requests directed to memory devices coupled to other memory hubs, the decoder being operable ~~and~~ to determine a memory request identifier associated with each memory request;

a packet memory coupled to the decoder, the packet memory being operable to receive memory request identifiers from the decoder and to store the received memory request identifiers;

a multiplexor being operable to couple either remote memory responses that are received responsive to the remote memory requests or local memory responses that are received responsive to the local memory requests to an output responsive to a control signal; and

arbitration control logic coupled to the multiplexor and the packet memory and being operable to determine from the memory request identifiers stored in the packet memory the recency of the memory requests corresponding to the received remote memory responses and the local memory responses and to generate the control signal based on the determination.

2. (Original) The memory hub of claim 1 wherein the arbitration control logic generates the control signal based on an oldest memory request identifier in the packet memory.

3. (Original) The memory hub of claim 1 wherein the packet memory is a first-in, first-out (FIFO) memory.

4. (Previously Presented) The memory hub of claim 1 wherein the arbitration control logic generates the control signal such that if an oldest memory request identifier stored in the packet memory is for a local memory request, the multiplexor outputs a local memory response.

5. (Original) The memory hub of claim 1 wherein each of the local and remote memory responses comprise data and a header identifying a memory request corresponding to the memory response.

6. (Previously Presented) A memory hub being operable to receive local memory responses and remote memory responses, the memory hub being operable to apply an arbitration algorithm to select the order in which the local and remote memory responses are provided on an uplink output based on the ages of memory requests corresponding to the local and remote memory responses.

7. (Original) The memory hub of claim 6 wherein the memory hub further comprises a packet memory that stores memory request identifiers in an order in which the corresponding memory requests are received.

8. (Original) The memory hub of claim 7 wherein the memory hub further comprises a multiplexer coupled to the packet memory, the multiplexor providing either a local or a remote memory response on an output responsive to a control signal.

9. (Original) The memory hub of claim 8 wherein the memory hub further comprises arbitration logic coupled to the packet memory and the multiplexer, and wherein the arbitration logic applies the control signal to the multiplexer to control which memory responses are provided on the output.

10. (Original) The memory hub of claim 6 wherein each of the local and remote memory responses comprise data and a header identifying a memory request corresponding to the memory response.

11. (Previously Presented) A memory module, comprising:

a plurality of memory devices; and

a memory hub coupled to the memory devices, the memory hub comprising:

a decoder adapted to receive memory requests including local memory requests directed to memory devices connected directly to the memory hub and remote memory requests directed to memory devices coupled to other memory hubs, the decoder being operable to determine a memory request identifier associated with each memory request;

a packet memory adapted to receive memory request identifiers and store the memory request identifiers;

a multiplexor adapted to receive remote memory responses that are responsive to the remote memory requests and local memory responses that are responsive to the local memory requests and being operable to select either the remote memory responses or the local memory responses in response to a control signal; and

arbitration control logic coupled to the multiplexor and the packet memory and being operable to determine from the memory request identifiers stored in the packet memory the recency of the memory requests corresponding to the received remote memory responses and the local memory responses and to generate the control signal to control selection of which memory response to output based on the determination.

12. (Original) The memory module of claim 11 wherein each of the memory devices comprise an SDRAM.

13. (Original) The memory module of claim 11 wherein the arbitration control logic generates the control signal based on an oldest memory request identifier in the packet memory.

14. (Original) The memory module of claim 11 wherein the packet memory is a first-in, first-out (FIFO) memory.

15. (Previously Presented) The memory hub of claim 11 wherein the arbitration control logic generates the control signal such that if an oldest memory request identifier stored in the packet memory is for a local memory request, the multiplexor outputs a local memory response.

16. (Original) The memory hub of claim 11 wherein each of the local and remote memory responses comprise data and a header identifying a memory request corresponding to the memory response.

17. (Previously Presented) A memory system, comprising:

a memory hub controller;

a plurality of memory modules, each memory module being coupled to adjacent memory modules through respective high-speed links, at least one of the memory modules being coupled to the memory hub controller through a respective high-speed link, and each memory module comprising:

a plurality of memory devices; and

a memory hub coupled to the memory devices, the memory hub comprising,

a decoder adapted to receive memory requests including local memory requests directed to memory devices connected directly to the memory hub and remote memory requests directed to memory devices coupled to other memory hubs, the decoder being operable to determine a memory request identifier associated with each memory request;

a packet memory adapted to receive memory request identifiers and store the memory request identifiers;

a multiplexor adapted to receive remote memory responses that are responsive to the remote memory requests and local memory responses that are responsive to the

local memory requests and being operable to select either the remote memory responses or the local memory responses in response to a control signal; and

arbitration control logic coupled to the multiplexor and the packet memory and being operable to determine from the memory request identifiers stored in the packet memory the recency of the memory requests corresponding to the received remote memory responses and the local memory responses and to generate the control signal to control selection of which memory response to output based on the determination.

18. (Original) The memory system of claim 17 wherein each of the high-speed links comprises an optical communications link.

19. (Original) The memory system of claim 17 wherein at least some of the memory devices comprise SDRAMs.

20. (Original) The memory system of claim 17 wherein the arbitration control logic generates the control signal based on the age of the memory request identifiers stored in the packet memory.

21. (Previously Presented) The memory system of claim 20 wherein the arbitration control logic generates the control signal such that if an oldest memory request identifier stored in the packet memory is for a local memory request, the multiplexor outputs a local memory response.

22. (Original) The memory system of claim 17 wherein the packet memory is a first-in, first-out (FIFO) memory.

23. (Original) The memory system of claim 17 wherein each of the local and remote memory responses comprise data and a header identifying a memory request corresponding to the memory response.

24. (Previously Presented) A computer system, comprising:

a processor;

a system controller coupled to the processor, the system controller including a memory hub controller;

an input device coupled to the processor through the system controller;

an output device coupled to the processor through the system controller;

a storage device coupled to the processor through the system controller;

a plurality of memory modules, each memory module being coupled to adjacent memory modules through respective high-speed links, at least one of the memory modules being coupled to the memory hub controller through a respective high-speed link, and each memory module comprising:

a plurality of memory devices; and

a memory hub coupled to the memory devices and coupled to the corresponding high-speed links, the memory hub including,

a decoder adapted to receive memory requests including local memory requests directed to memory devices connected directly to the memory hub and remote memory requests directed to memory devices coupled to other memory hubs, the decoder being operable to determine a memory request identifier associated with each memory request;

a packet memory adapted to receive memory request identifiers and store the memory request identifiers;

a multiplexor adapted to receive remote memory responses that are responsive to the remote memory requests and local memory responses that are responsive to the local memory requests and being operable to select either the remote memory responses or the local memory responses in response to a control signal; and

arbitration control logic coupled to the multiplexor and the packet memory and being operable to determine from the memory request identifiers stored in the packet memory the recency of the memory requests corresponding to the received remote memory responses and the local memory responses and to generate the control signal to control selection of which memory response to output based on the determination.

25. (Original) The computer system of claim 24 wherein each of the high-speed links comprises an optical communications link.

26. (Original) The computer system of claim 24 wherein at least some of the memory devices comprise SDRAMs.

27. (Original) The computer system of claim 24 wherein the processor comprises a central processing unit (CPU).

28. (Original) The computer system of claim 24 wherein each of the local and downstream memory responses comprise data and a header identifying a memory request corresponding to the memory response.

29. (Previously Presented) In a memory system including a plurality of memory modules, each memory module including a memory hub coupled to memory devices, a method of processing and forwarding memory responses in the memory hub of each memory module, comprising:

receiving memory requests, each having a memory request identifier, the memory requests including local memory requests directed to memory devices connected to the memory hub and remote memory requests directed to memory devices coupled to memory hubs in other memory modules;

storing the memory request identifiers;

storing local memory responses received from the memory devices in response to the local memory requests;

storing remote memory responses received from the other memory modules in response to the remote memory requests;

applying in at least one hub an arbitration algorithm based on the ages of the stored memory request identifiers to determine an order in which the stored local and remote memory responses are forwarded; and

forwarding the local and remote memory responses upstream according to the determined order.

30. (Original) The method of claim 29 wherein each of the local and remote memory responses comprise data and a header identifying a memory request corresponding to the memory response.

31. (Original) The method of claim 29 further comprising generating a control signal to indicate the order based on an oldest stored memory request identifier.

32. (Original) The method of claim 29, wherein the memory request identifiers are stored and accessed on a first-in, first-out (FIFO) basis.

33. (Original) The method of claim 29, further comprising generating a control signal such that if an oldest stored memory request is a local memory request, a local memory response is forwarded.

34. (Currently Amended) The memory hub of claim 1, further comprising a packet tracker coupled to the packet memory, the packet memory being operable to receive the remote memory responses and to associate each received remote memory response with a memory request identifier stored in the packet memory, the packet tracker being operable to cause the memory request identifier to be ~~effectively~~ removed from the packet memory.

35. (Currently Amended) The memory module of claim 11, further comprising a packet tracker adapted to receive the remote memory responses and being operable to associate each remote memory response with a memory request identifier stored in the packet memory and remove the associated memory request identifier from the packet memory.

36. (Currently Amended) The memory system of claim 17, further comprising a packet tracker adapted to receive the remote memory responses and being operable

to associate each remote memory response with a memory request identifier stored in the packet memory and remove the associated memory request identifier from the packet memory.

37. (Currently Amended) The computer system of claim 24, further comprising a packet tracker adapted to receive the remote memory responses and being operable to associate each remote memory response with a memory request identifier stored in the packet memory and remove the associated memory request identifier from the packet memory.